

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		10/365,067
Filing Date		2006-11-30
First Named Inventor	J.D. Chipala et al.	
Art Unit	2821	
Examiner Name	TUYET VO	
Attorney Docket Number	Chipala 11-11	

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
TV	1	S. TAM ET AL., "Clock Generation and Distribution for the First IA-64 Microprocessor," IEEE Journal of Solid-State Circuits, Vol. 35, No. 11, November 2000, pp. 1545-1552.	<input type="checkbox"/>
I	2	TED KEHL, "Hardware Self-Tuning and Circuit Performance Monitoring," In Proc. IEEE International Conference on Computer Design: VLSI in Computers and Processors, 1993, pp. 188-192.	<input type="checkbox"/>
	3	Y. ELBOIM ET AL., "A Clock-Tuning Circuit for System-on-Chip," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 11, No. 4, August 2003, pp. 616-626	<input type="checkbox"/>
	4	N. TIWARI ET AL., "Skew Generation and Analysis in Timing-Critical Circuits," EDN (www.edn.com), November 13, 2003, pp. 87-96.	<input type="checkbox"/>
	5	K. RAHIMI ET AL., "In-Circuit Self-Tuning of Clock Latencies," Proceedings of the Sixth International Symposium on Quality Electronic Design (ISQED '05), 2005, 6 pages.	<input type="checkbox"/>
TV	6	S. TAM ET AL., "Clock Generation and Distribution for the 130-nm Itanium 2 Processor with 6-MB On-Die L3 Cache," IEEE Journal of Solid-State Circuits, Vol. 39, No. 4, April 2004, pp. 636-642.	<input type="checkbox"/>

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